ABSTRACT OF THE DISCLOSURE

A processor with a register renaming function comprises: an instruction fetch; a decoder for an instruction code of a fetched instruction; a register holding data corresponding to a register number; a register body holding data corresponding to a register number; a caching register to cache the contents in the body; an inner instruction information holder (IIIH) to hold information on a state of an inner instruction including a logical register number and a caching register number of the caching register by the fetched instruction; an instruction insertion determiner (IID) to compare an instruction code by pre-decoding the fetched instruction with information on a state of the inner instruction of IIIH to determine the inner instruction; and a register transfer instruction issuer for transferring inner data between the caching register and the body when the IID determines the inner transfer instruction is to be inserted.